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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,254	04/21/2005	Chris Speirs	CH02 0033 US	8626
65913 NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131	7590 01/26/2009		EXAMINER MCCOMMAS, STUART S	
			ART UNIT 2629	PAPER NUMBER
		NOTIFICATION DATE 01/26/2009	DELIVERY MODE ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

[ip.department.us@nxp.com](mailto:ip.department.us@nxp.com)

<b>Office Action Summary</b>	<b>Application No.</b> 10/532,254	<b>Applicant(s)</b> SPEIRS, CHRIS
	<b>Examiner</b> Stuart McCommas	<b>Art Unit</b> 2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 17 November 2008.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1,2 and 4-7 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-2 and 4-7 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/DS/06)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/17/2008 has been entered.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al. (United States Patent 6,907,314), hereinafter referenced as Negishi, in view of Liang (WO 01/54108 A1), hereinafter referenced as Liang.

Regarding claim 1, Negishi discloses a display device comprising:

a plurality of pixels arranged in an array having n rows and m columns (figure 4), each of said pixels comprising:

a switching element having a gate (figure 4);

a capacitor coupled to said switching element (figure 4);

control lines and data lines that select said pixels (figure 4);

a row driver circuit (10) that activates each pixel in the n rows by means of a row voltage applied to said gate of said switching element (figure 4; figure 8);

a column driver circuit that controls the m columns with column voltage, said column voltage corresponding to image data of the pixels of selected row to be displayed (column 10 lines 34-51; figure 4), where the capacitor is charged with voltages for the pixel (figure 4; figure 8).

However Negishi fails to disclose a display device that reduces energy consumption wherein during a transition from a selected row n to another row n+x, the capacitor is charged with an intermediate voltage level during discharging of row n and row n+x is charged with said intermediate voltage level by said capacitor after the row voltage of row n is fully discharged.

In a similar field of invention Liang discloses a display device that reduces energy consumption wherein during a transition from a selected row n to another row n+x, the capacitor is charged with an intermediate voltage level during discharging of row n and row n+x is charged with said intermediate voltage level by said capacitor after the row voltage of row n is fully discharged to an intermediate voltage with the capacitor disclosed in page 4 lines 1-33 and in page 5 lines 1-5 and in page 10 lines 25-31 and in page 11 lines 1-19 and exhibited in figure 1 and in figure 3 and in figure 5.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Negishi with Liang by specifically providing a display device that reduces energy consumption wherein during a transition from a selected row n to another row n+x, the capacitor is charged with an intermediate voltage level during

discharging of row n and row n+x is charged with said intermediate voltage level by said capacitor after the row voltage of row n is fully discharged for the purpose of providing a display that saves power by using charge sharing (page 4 lines 13-20).

Regarding claim 2, Negishi and Liang, the combination discloses everything as applied above, further Liang discloses that a plurality of intermediate voltage levels are provided for charge sharing, and the selected row n can be coupled in steps to a first intermediate voltage level and subsequently to further intermediate voltage levels up to a final intermediate voltage level for the purpose of charge sharing disclosed in page 4 lines 9-19 and in page 10 lines 7-31 and in page 11 lines 1-13 and exhibited in figure 3 and in figure 5.

Regarding claim 4, Negishi and Liang, the combination discloses everything as applied above (see claim 1), further Liang discloses that the maximum column voltage is an intermediate voltage level which reads on claimed "a maximum column voltage is used as the intermediate voltage level" disclosed in page 8 lines 21-33 and in page 17 lines 15-25 and exhibited in figure 2 and in figure 5.

Regarding claim 5, Negishi and Liang, the combination discloses everything as applied above, further Liang discloses that the intermediate row voltage is at half of the row voltage which reads on claimed "that a voltage corresponding to the intermediate voltage level is half of the applied row voltage" disclosed in page 4 lines 13-19 and exhibited in figure 2 and in figure 5.

Regarding claim 6, Negishi and Liang, the combination discloses everything as applied above, further Liang discloses that a switching unit is provided for switching the

first row and then a row n+x to the intermediate voltage level which reads on claimed "that a switching unit is provided for first connecting the selected row n, and subsequently the row n+x to the intermediate voltage level" disclosed in page 10 lines 7-31 and in page 11 lines 1-18 and exhibited in figure 3 and in figure 5.

Regarding claim 7, Negishi a method used for a display device with pixels arranged in rows n and column m, each pixel comprising a capacitor coupled to a switching element (figure 4), said method comprising the following steps:

supplying row voltages to the rows via control lines to select said rows (column 10 lines 5-50; figure 4; figure 8);

supplying column voltage to the columns m via data lines and charging said capacitor (column 10 lines 5-50; figure 4; figure 8),

However Negishi fails to disclose a method of reducing energy consumption during row transitions in a display device, and during a transition from a selected row n to another row n+x, charging the capacitor to an intermediate voltage level during discharging of selected row n, and charging row n+x to said intermediate voltage level with said capacitor after the row voltage of row n is fully discharged.

In a similar field of invention Liang discloses a method of reducing energy consumption during row transitions in a display device where during a transition from a selected row n to another row n+x, charging the capacitor to an intermediate voltage level during discharging of selected row n, and charging row n+x to said intermediate voltage level with said capacitor after the row voltage of row n is fully discharged to an intermediate voltage level with the capacitor disclosed in page 4 lines 1-33 and in page

5 lines 1-5 and in page 10 lines 25-31 and in page 11 lines 1-19 and exhibited in figure 1 and in figure 3 and in figure 5.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Negishi with Liang by specifically a method of reducing energy consumption during row transitions in a display device where during a transition from a selected row n to another row n+x, charging the capacitor to an intermediate voltage level during discharging of selected row n, and charging row n+x to said intermediate voltage level with said capacitor after the row voltage of row n is fully discharged for the purpose of providing a display that saves power by using charge sharing (page 4 lines 13-20).

***Response to Arguments***

6. Applicant's arguments with respect to claims 1-2 and 4-7 have been considered but are believed to be answered by and therefore moot in view of the new ground(s) of rejection.

On pages 6-7 of Applicant's remarks, Applicant argues that Liang does not disclose waiting to fully discharge the row n during the precharging.

The Examiner respectfully disagrees, because Liang discloses that the row voltage of row n is fully discharged to an intermediate voltage level with the capacitor when the charge sharing is performed disclosed in page 4 lines 1-33 and in page 5 lines 1-5 and in page 10 lines 25-31 and in page 11 lines 1-19 and exhibited in figure 1 and in figure 3 and in figure 5.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571)272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/  
Supervisory Patent Examiner, Art Unit 2629

Stuart McCommas  
Patent Examiner  
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SSM